Design and Verification of the Second-Generation Precipitation Radar Processor/Controller

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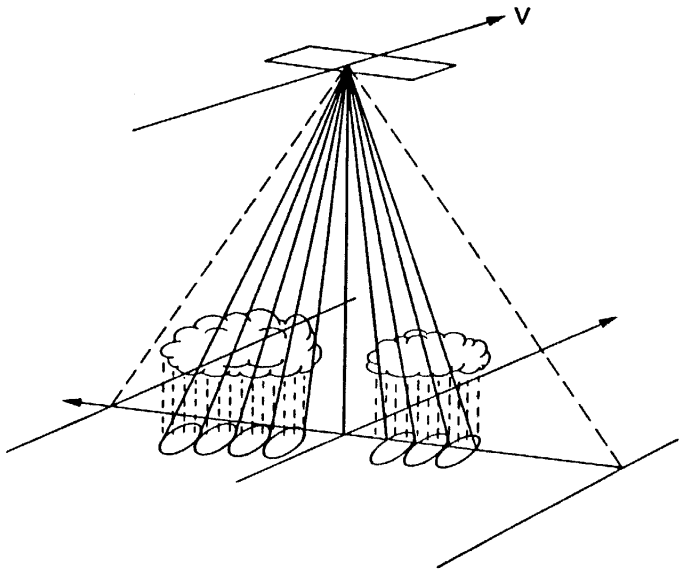


Overview

- Observation requirements for an advanced, global rain measuring mission
- PR-2 (Second-Generation Precipitation Radar) adaptive scanning approach
- FPGA-based design of the ultra-high throughput Data Processor
- Test results and TRL summary for the space-grade processing hardware

Requirements for an advanced rain radar mission

Measuring detailed structure of rainfall on a global scale

Plans for Global Precipitation Measurement mission: Dual-Frequency Precipitation Radar

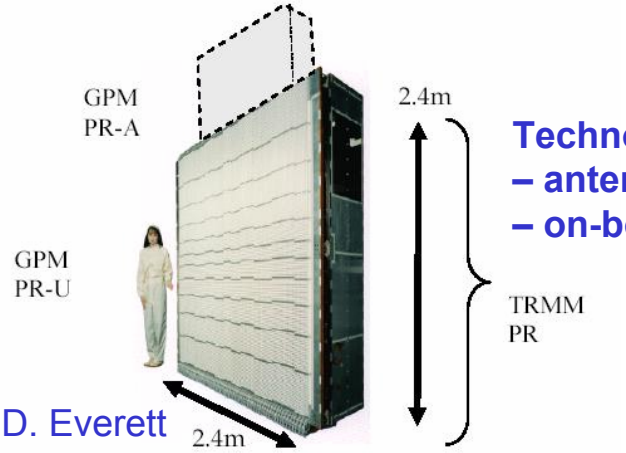
Ku/Ka-band (14 and 36 GHz)—inherited technology from Tropical Rainfall Measuring Mission

The need for enhanced observation capabilities (resolution and swath width)

NASA/JPL development of an innovative on-board processor for the Second-Generation Precipitation Radar (PR-2—a follow-on to GPM)

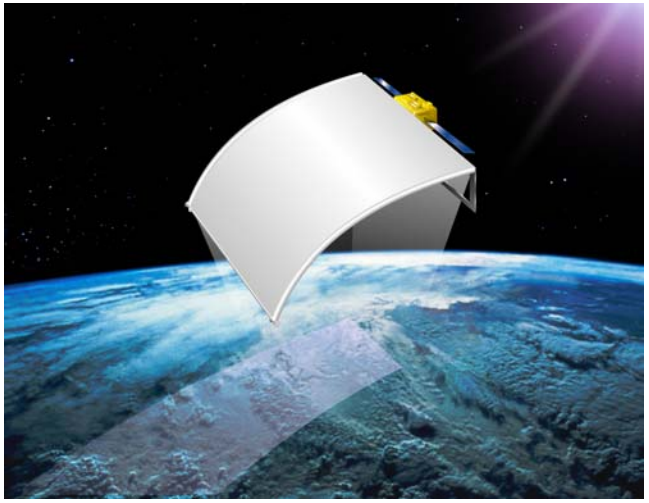
– Autonomous radar with adaptive scanning and science data compression

– High-density, rad-tolerant field-programmable gate array design



(from D. Everett et al., 2002)

Technology breakthroughs:
– antenna
– on-board processing



GPM Dual-Frequency Precipitation Radar (DPR)
2.4×2.4 m antenna aperture
conventional slotted waveguide/phased array
5 km resolution, 200 km swath

Second-Generation Precipitation Radar (PR-2)
5.3×5.3 m antenna aperture
Inflatable/rigidizable reflector with linear array feed
2 km resolution, 500 km swath

Adaptively scanning radar

- Rainfall science data reduction is needed to achieve wide swaths (500 km) and high horizontal spatial resolution (2 km).
  - PR-2 has a 10-fold increase in number of radar beam locations compared to TRMM or GPM
  - Dwell time limits: $N \geq 60$ independent radar looks needed per beam for accurate rainfall measurements.
  - Sparseness of rainfall suggests an auto-targeting solution.
- Adaptive scanning innovation for PR-2
  - Built-in intelligence to auto-target areas of rain
  - Sweep sequence: locator sweep, beam sort algorithm, high-resolution sweep
  - Uniqueness from conventional, fixed PRF scanning method
- Counting problem: How to generate a reliable transmit/receive timing solution for the PR-2's electronically steerable array
  - Requires beam steering sequence and PRI variation to maximize independent looks
  - Requires on-the-fly timing of transmit/receive pulses, without any collisions.

Adaptive scan timing solution

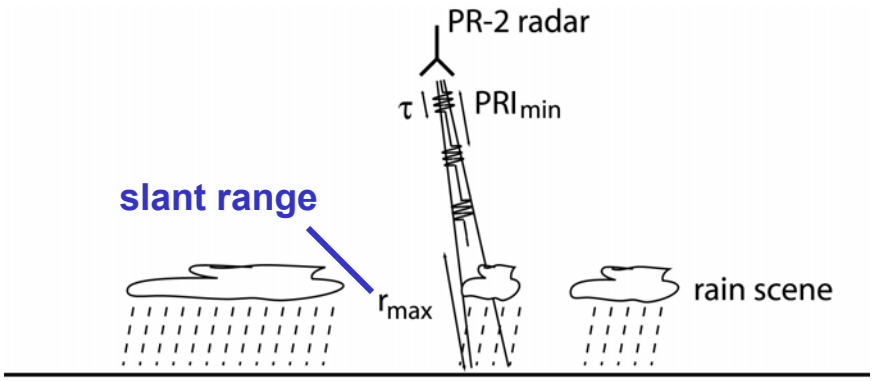
After beam sequence is determined:

- **EIF build-up phase (transmit only)**

$$\text{minimum } PRI = 2\tau + 2r_{\max}/c$$

$$EIF = \text{floor}\left(t_{range-delay(\min)}/PRI_{\min}\right)$$

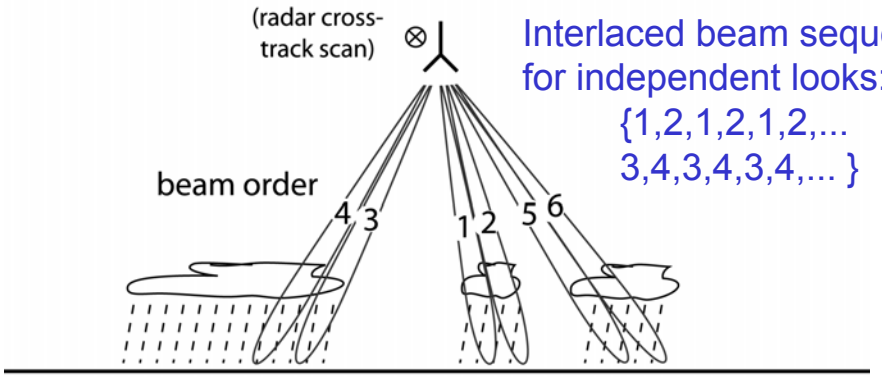
(constant throughout sweep)



- **Closed loop transmit/receive**

  Tx pulses follow falling edge of Rx echo

  Beam sequence moves nadir-to-side (monotonically increasing PRI)

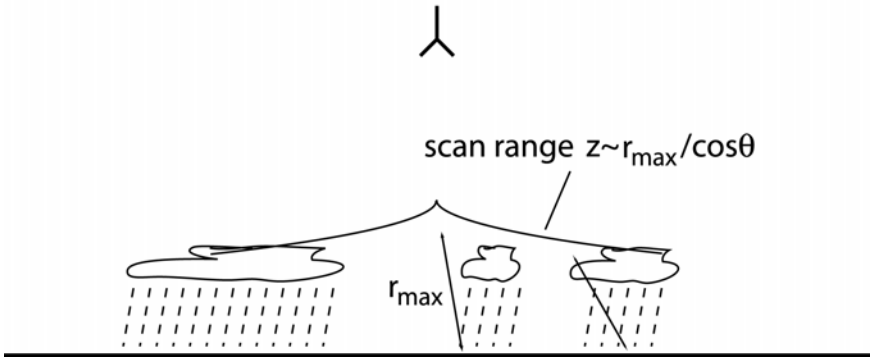


Interlaced beam sequence for independent looks:
{1,2,1,2,1,2,...
3,4,3,4,3,4,... }

- **Rx window held constant throughout sweep**

(defined by maximum slant altitude r_{max})

r_{max} = 8 km altitude for locator sweep
12 km altitude for hi-res sweep



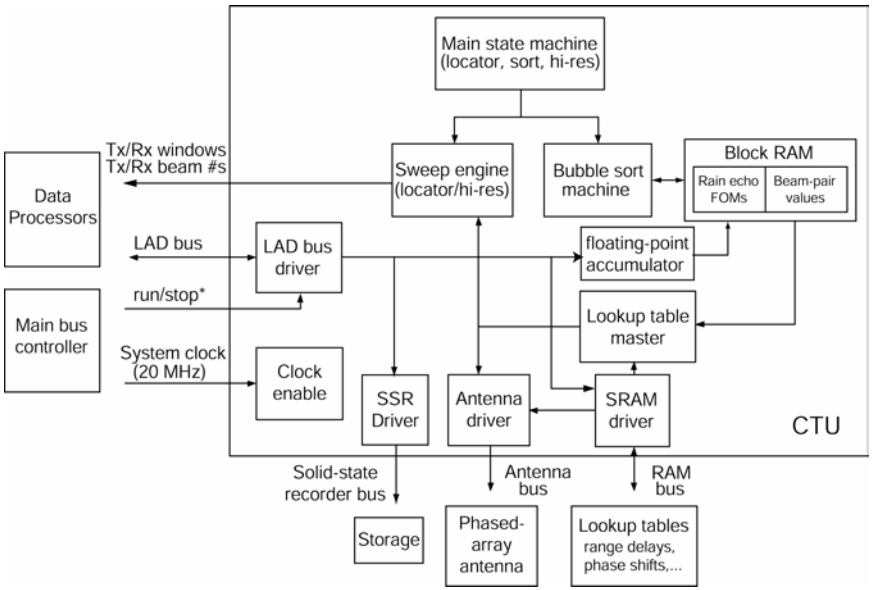
Control and Timing Unit (CTU) Design

Implemented adaptive scan control algorithm onto one Xilinx Virtex FPGA

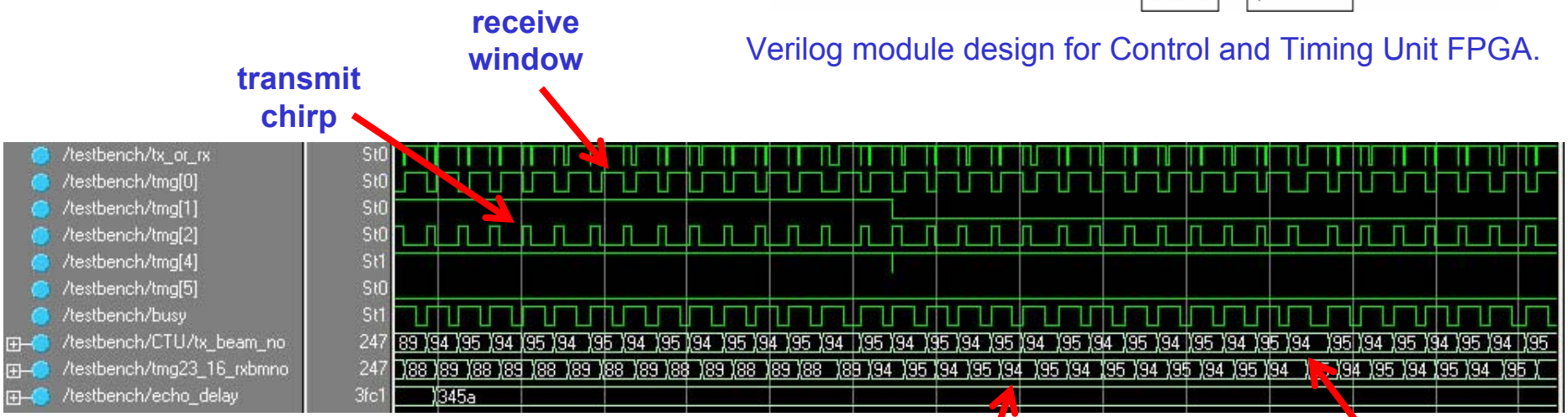
Custom state-machine architecture to handle time critical Tx/Rx operations

Latest version performs full 500 km (250 beam) adaptive scan sequences

– Default setting: 10% of quick-look beams are selected for hi-res sweep



Verilog module design for Control and Timing Unit FPGA.



Verilog simulation of CTU output during high-resolution sweep.

Timing efficiency results for CTU

Timing efficiency--percentage of total sweep time dedicated to transmit/receive pulses.

Measured for various rain profiles in Verilog simulation and in actual hardware operation:

Best case All heavy rain located near nadir beam (very little range delay variation)

Random case Rainfall uniformly distributed over swath (45 dB max variation in reflectivity)

Worst case Minimal rain at nadir beam—rest of rain at extreme left and right edges of swath (large range delay variation between beams)

Results:

rain profile	total scan time	timing efficiency
worst case	277.5 ms	82.9%
random	260.0 ms	88.5%
best case	245.3 ms	93.7%

- 6-7 fold increase in independent looks per rain bin
- Flexibility with CTU numeric registers: trades between swath covervage and number of radar looks

PR-2 Data Processor

FPGA-based Data Processor design

Pulse-compression of linear FM chirp echoes

Implemented onto 2 rad-tolerant Xilinx Virtex-1000 FPGAs

40×10^9 op/s peak throughput for simultaneous processing of 4 receive channels (14 and 36 GHz, co- and cross-pol)

Large $B\tau$ product (~200) for increased independent radar looks, increased SNR

Successful demonstration aboard airborne PR-2 prototype deployments

– CAMEX-4 (Aug-Sept 2001)
– Wakasa Bay (Jan-Feb 2003)
– LRR Validation (May-June 2003)

PR-2 processor console

New features of spaceborne Data Processor FPGAs

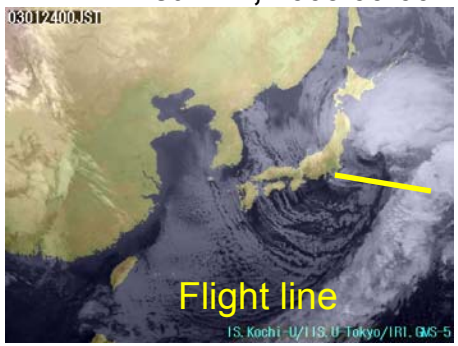
32-bit floating point accumulators for improved dynamic range

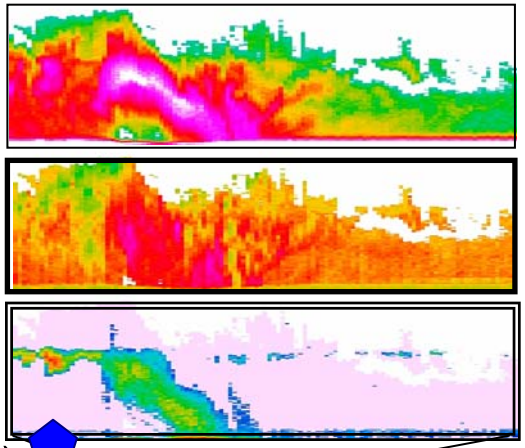
Crossbar memory drivers to accommodate staggered beam sequence (adaptive scan)

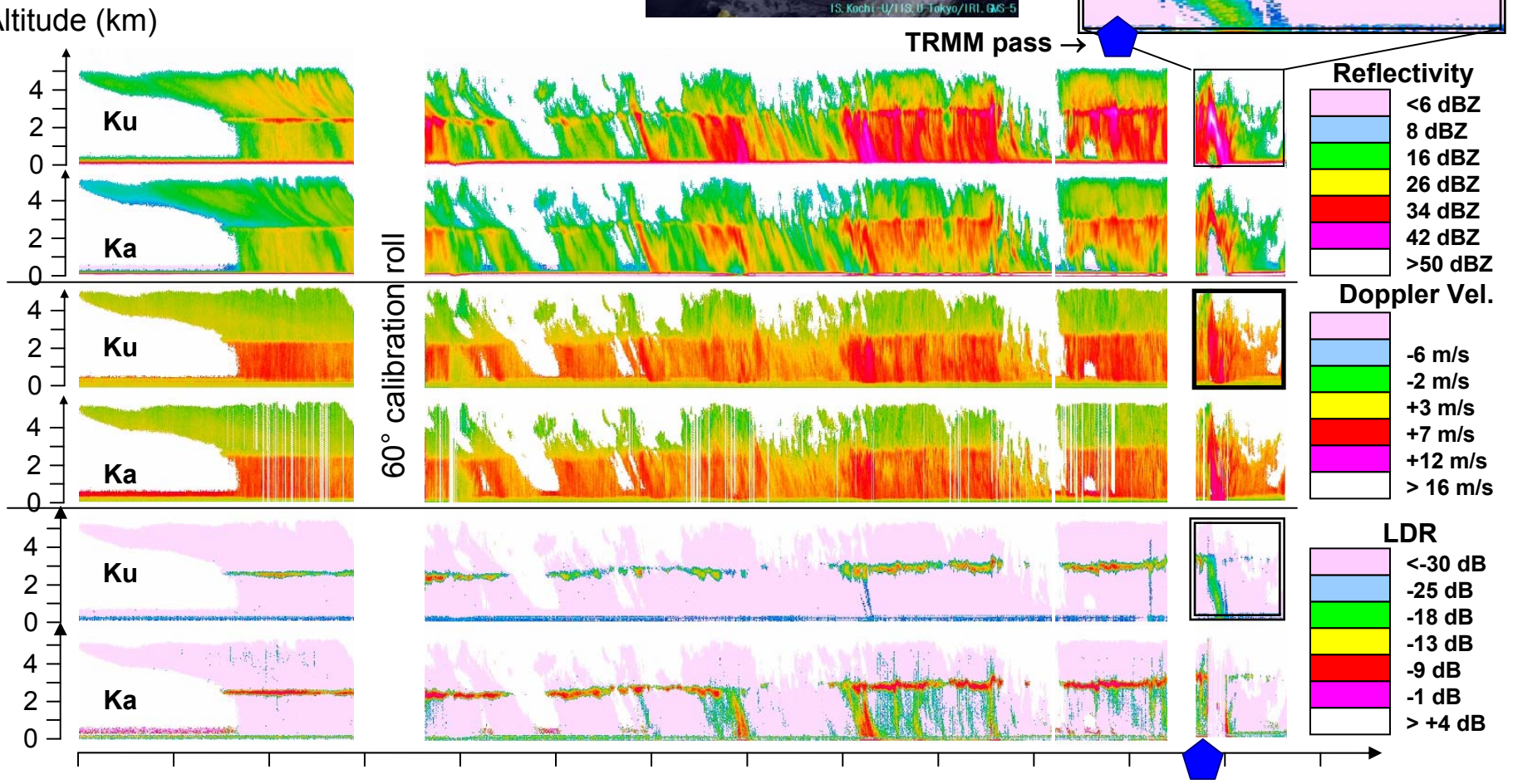
40 MB/s local address/data bus for fast data burst transfer to CTU

Airborne Data Processor demonstration in AMSR-E validation experiment, Japan

Data products c/o Simone Tanelli, JPL.

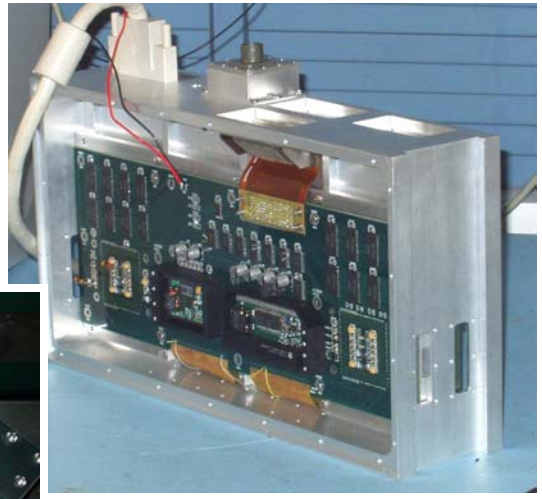


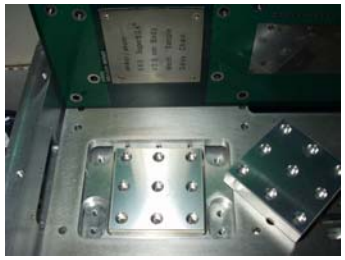




Test results for space-grade PR-2 hardware

- Completed design and assembly of PR-2 processor/controller module
- Design for space environment
  - All S-class equivalent parts (Virtex and Actel FPGAs, SRAM, buffers)
  - Configuration memory scrubbing for single-event upset recovery
  - Chassis design: Conductive cooling of Data Processor FPGAs





Space-grade chassis with assembled printed circuit boards.

Benchtop testing and installation in thermal chamber.

Experimental setup

- Designed benchtop PC data acquisition and control system
  - LabView GUI software + 32-bit digital I/O interface
- Testing with a target simulator (chirp waveform generator)
  - Can run entire adaptive scan cycles in real time
  - Processor operation confirmed in thermal chamber tests over –20 to +70 °C

Pulse-compressed output

Range sidelobe performance tests:

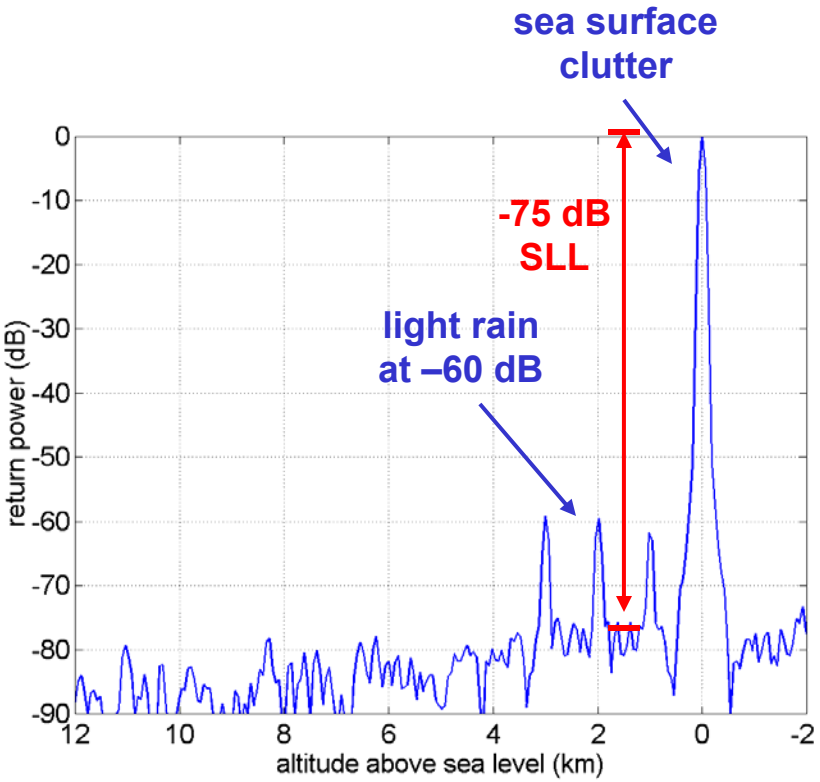
- FPGA Processor hardware operating in free-running mode.
- Offset video input from custom-made chirp waveform generator. (Simulates PR-2 observations at nadir with light rain targets over ocean.)

Conditions

- Rain scatterers 60 dB down (~1 mm/hr rain rate) at 1, 3, and 5 km altitude
- Chirp pulse: τ = 51 μs, B = 4 MHz, Hamming window taper
- Input signal quantization: 12-bit resolution, $\pm$1/2 LSB quantization noise
- 2x averaging in range (60 m vertical sampling)

Results

- -75 dB range sidelobes attainable from sea surface return
- → ***High detection sensitivity: even very weak scatterers (1 mm/hr rainfall) are discernable over sea surface clutter***



Power detected output from FPGA Data Processor hardware during free-running operation. (Target = ocean surface return + light rain scatterers at 1, 2, and 3 km.)

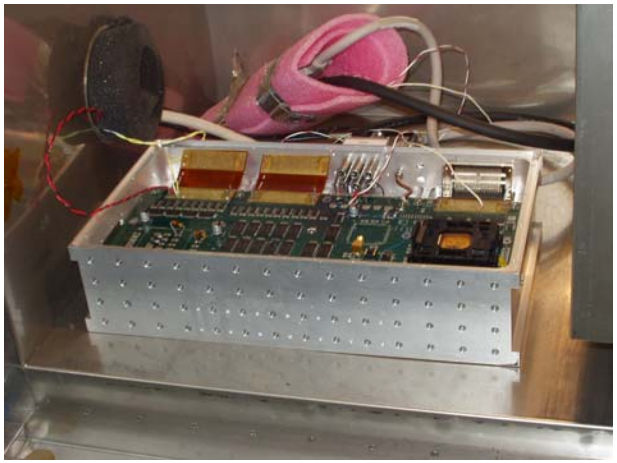
Power and thermal characterisitics

Thermal chamber testing of the PR-2 processor

- Measured chassis load currents and FPGA die junction temperatures (T_J)
- Tested over T_A = –20 to +70 °C ambient temperature range
- Calculated Data Processor power consumption at full throughput rate (20×10^9 op/s per chip)

Chassis thermal resistance calculations: $\theta_{JA} = (T_J - T_A)/P_{DP}$

Power and thermal summary:



Data Processor power consumption / temperature	**P_{DP} = 14.8 W per chip**, T_J = 35.1 °C (at 25 °C ambient)
Data Processor junction-to-air thermal resistance	**θ_{JA} = 0.68 °C/W** (mounted in chassis)
CTU power consumption	P_{CTU} = 1.0 W
chassis quiescent power	P_Q = 12.3 W
chassis operating power (full throughput)	$2P_{DP}+P_{CTU}+P_Q$ = **42.9 W**

- Power consumption defines baseline instrument requirements.
- Low θ_{JA} indicates efficient removal of heat from Data Processors. (Note typical θ_{JC}=0.8 °C/W for V-1000 BGA package.)
- High device reliability: At T_A=70°C, T_{Jmax} = 83.0°C (below 85°C design constraint for space-grade FPGAs).

Error detection and correction (EDAC)

- Susceptibility of SRAM-technology FPGAs (e.g., Xilinx Virtex series parts) to radiation upsets in space
- EDAC approach for single-event upsets
  - Hamming code appended to each data word in configuration memory
  - Memory scrubbed with rad-tolerant Actel FPGA
  - Periodic (5 min.) reconfiguration of Virtex FPGAs
  - Advantages over triple module redundancy schemes
- EDAC reliability tests
  - PR-2 processor/controller was tested repeatedly in the thermal chamber with software-induced bit errors (T_A = 25, 40, 50, 60, 70, and –20 °C).
  - In all cases, FPGAs successfully recovered from bit flips upon next configuration cycle.

TRL summary for the PR-2 satellite processor/controller

Aspect of design	TRL at project start	Present TRL
On-board processing and science data compression	5	6
Timing solution for auto-targeting of rain	2	5
FPGA-based control of spaceborne instrument	2	5
Radiation upset correction approach	2	5

Findings:

- Timing efficiency for auto-targeting of rain confirmed at 83-94% of scan time
- Range sidelobe performance of –75 dB achieved using FPGA receive processor design
- Power budget: 15 W per data processor chip, 43 W for entire on-board processor
- Built-in EDAC tested successfully in presence of bit flips
- Chassis conductive cooling proven effective in thermal chamber tests

  – *Results establish baseline instrument requirements and capabilities for an advanced rain radar mission.*